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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,908	07/24/2006	Akihiro Goto	1032404-000154	1812

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
08/01/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/586,908	GOTO ET AL.	
	Examiner	Art Unit	
	NGHIA M. DOAN	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) *11 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Application 10/586,908 filed on 06/30/2006. Claims 11-20 remain pending. Claims 1-10 have been canceled.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species:

Species I: claims 11-12, drawn in figure 15, which a design support wiring design for bond wire, without design rule considered and package data involved.

Species II: claims 13-20, drawn in figure 1, which a design support wiring design for bond wire and taking design rule into considered and package data involved.

The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, there has no generic.

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election of the species may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species.

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.

3. During a telephone conversation with Mr. James A. LaBarre (Reg. 28,632) on July 24th, 2008 for a provisional election was made with traverse to prosecute the invention of Species II, claims 13-20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-12 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

5. Claims 13-20 are to be examined in this office action and the non-elected claims 11-12 should be canceled in the next communication

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: -- wiring design support apparatus for bond wire of a semiconductor devices --.

Drawings

7. The drawings are objected to because Figure 1 is required to label or delete input and output of blocks [2] and [9], respectively. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. As respect to claim13, recited the limitation "fluctuation arrangement" which renders the claim indefinite because it is unclear what "fluctuation" means and roles and how to specify/evaluate "fluctuation" in the claimed invention. See MPEP § 2173.05(d).

11. As respect to claim13, recited the limitation "an arranging the semiconductor chip on an interposer" which render the claim indefinite because it is unclear where "an interposer" is located, is it belong or part of a semiconductor chip or is it off (e.g., excluded) from a semiconductor chip? The claimed invention does not provide or specify where "an interposer" is come from? How "an interposer" would be effect to the semiconductor chip's position and bond wire? Furthermore, "an interposer position", Is it fixed location or to be changeable? (note: an interposer located will give a different design constraint, such as if it is "fixed", then "semiconductor chip location" to be constraint. Otherwise, both "interposer location" and "semiconductor chip location" to be constraint. Hence, Examiner could not determine whether which "design constraint" will be accountable in the claimed invention.

As unclear issue above, Examiner position that one end of a bond wire connected to a semiconductor chip and the other end of the bond wire connect to anything which is treated as "an interposer" and "the semiconductor chip" can be freely located or position and be connected to "bond wire".

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ding et al., (US Pat. 5,801,959) (see entire document).

14. With respect to claim 13, Ding discloses a design support apparatus (e.g., system) for an integrated circuit layout (the abstract) comprising:

a first data creating unit that creates, based on design data of a semiconductor package, semiconductor chip simulated arrangement data obtained by arranging a semiconductor chip in a position where fluctuation in an arrangement position of the semiconductor chip in arranging the semiconductor chip on an interposer is simulated (determining location and/or placing component(s) on die surface is determined) (col. 1, ll. 12-27, col. 2, ll. 47-65, col. 3, ll. 1-2, col. 4, ll. 44-50, see fig. 1, step [101] and fig. 3, step [301], fig. 8, step [801] [803] [804]);

a second data creating unit that creates, based on the design data of the semiconductor package and the semiconductor chip simulated arrangement data, bond wire (e.g., interconnection) simulation data obtained by wiring (e.g., interconnection),

using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate (changing and/or adjustable) from an arrangement position in the design data (relocate component) (fig. 8, step [804]) and bond wire connection terminals of the interposer (relocate I/O cell) (fig. 8, step [810]) (the interconnection between pins of components are routed) (see fig. 1, step [102] [103], fig. 2B, fig. 3, step [302] [303], col. 4, line 51 - col. 5, line16, col. 6, line 48 - col. 7 line 10 and also see fig. 6 and fig. 8, steps [802] [805] [806] [810], col. 12, ll. 17-31);

a measuring unit that measures (e.g., estimate, defines) a design rule for the bond wires (e.g., routing constraint or resource) used for the wiring from the bond wire simulation data (col. 8, ll. 1-58); and

an analyzing (evaluating) unit that analyzes measurement result obtained by the measuring unit (fig. 11, col. 12, ll. 12-31 and ll. 40-54, col. 13, ll. 20-33).

15. With respect to claim 14, Ding discloses wherein the design data of the semiconductor package includes shape of the interposer (varies sizes given a shape), shape of the semiconductor chip (varies size of cell or block or component given shape), an arrangement position of the semiconductor chip on the interposer, shape (routing channel width and/or height given shape) of the bond wires that connect the semiconductor chip and the interposer (col. 8, line 1 - col. 9, line. 18), and arrangement positions of the bond wires that connect the semiconductor chip and the interposer (col. 10, ll. 1-35).

16. With respect to claim 15, Ding discloses wherein the first data creating unit creates semiconductor chip simulated arrangement data obtained by arranging, with

respect to the arrangement position of the semiconductor chip on the interposer in the design data of the semiconductor package, the semiconductor chip in a position where fluctuation in an arrangement position of the semiconductor chip in an in-plane direction or a rotation direction on a semiconductor chip arrangement surface of the interposer or fluctuation in inclination of the semiconductor chip in a thickness direction of the interposer is simulated (an in-plane direction) (col. 10, ll. 43-58, col. 12, ll. 40-54).

17. With respect to claim 16, Ding discloses wherein the measuring unit measures clearance between the bond wires and clearance between the bond wires and the semiconductor chip as the design rule (col. 8, line 1 - col. 9, line. 18).

18. With respect to claim 17, Ding discloses wherein the analyzing unit analyzes a tolerance of fluctuation in an arrangement position of the semiconductor ship on the interposer that satisfies the design rule (col. 8, line 1 - col. 9, line. 18).

19. With respect to claim 18, Ding discloses wherein the analyzing unit analyzes a tolerance of fluctuation in bond wire connection terminal positions of the interposer that satisfies the design rule (col. 8, line 1 - col. 9, line. 18).

20. With respect to claim 19, Ding discloses comprising a storing unit that stores therein the measurement result (output) (fig. 11, col. 12, ll. 12-31 and ll. 40-54, col. 13, ll. 20-33).

21. With respect to claim 20, Ding discloses comprising a storing unit that stores therein analysis result obtained by the analyzing unit (fig. 11, col. 12, ll. 12-31 and ll. 40-54, col. 13, ll. 20-33).

22.

23. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Razon et al., (US 5,950,070) (see entire document).

24. With respect to claim 13, Razon discloses a method and tool (apparatus) used in formatting the chip scale package (the abstract an col. 1, ll. 6-8), comprising:

a first data creating unit that creates, based on design data of a semiconductor package (contact patterns, bond pads, interposer location, bond wiring, solder ball lands etc.), semiconductor chip simulated arrangement data obtained by arranging a semiconductor chip in a position where fluctuation in an arrangement position of the semiconductor chip in arranging the semiconductor chip on an interposer is simulated (alignment chip on the interposer controls whether each one of the electrical connection (e.g., bondwires) between terminals of the interposer and the contacts of the chip can be made successfully without great difficulty) (the abstract, col. 3, ll. 1-13, col. 5, ll. 24-43, col. 7, ll. 8-15);

a second data creating unit that creates, based on the design data of the semiconductor package (contact patterns, bond pads, interposer location, bond wiring, solder ball lands etc.) and the semiconductor chip simulated arrangement data, bond wire simulation data obtained by wiring, using bond wires, the bond wire connection terminals of the semiconductor chip arranged to deviate (e.g., relaxed, change, loose, tolerance, or adjustable) from an arrangement position in the design data and bond wire connection terminals of the interposer (the abstract, col. 3, ll. 16-31, col. 5, ll. 49-64, col. 6, line 63 - col. 7, line 22, col. 7, ll. 45-54, col. 8, ll. 12-23);

a measuring unit that measures a design rule (predetermined of acceptance criteria such as: minimum pitch between adjacent solder ball lands and allow the greatest number of interconnections or bond wires per unit area or angle of wiring direction) for the bond wires used for the wiring from the bond wire simulation data (col. 4, ll. 56-62, col. 6, ll. 6-12, col. 7, ll. 8-15 and ll. 45-54); and

an analyzing unit that analyzes measurement result obtained by the measuring unit (col. 4, ll. 31-43, col. 7, ll. 15-22, ll. 45-51 col. 8, ll. 12-23).

25. Claims 13-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Howard et al., (US Pat. 7,132,359) (see entire document).

26. With respect to claims 13-20, Howard discloses a wirebonding methods wherein bondwires are positioned using dynamically determined variations in die (chip or semiconductor device) include steps for placing a die on the prepared substrate using selected ideal placement coordinates (position) in (x-y coordinates) . Deviation of the actual die (chip or semiconductor device) (dx; dy) from the selected ideal placement coordinates is monitored, and one or more critical bondwires are wirebonded between respective die pins and pins on the substrate (interposer). The monitored (measured) placement deviation (dx;dy) is used to dynamically position the critical wirebonds on the critical pins according to actual die placement that using lateral deviation monitoring and angular deviation monitoring to dynamically position wirebonds (see entire document)

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGHIA M. DOAN whose telephone number is (571)272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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07/28/2008